

CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor device package (50, 102, 110) comprising:
a molding compound (54) forming at least a portion of a first package face (56);
a semiconductor device (14) at least partially covered by the molding compound (54),
5 the semiconductor device (14) including a plurality of I/O pads (80); and
a lead frame (52, 100, 112) of electrically conductive material at least partially covered
by the molding compound (54), the lead frame (52, 100, 112) including a plurality of leads
(60), each of the leads (60) including:
an interposer (64) having opposing first and second ends (66, 68), the interposer
10 (64) being spaced apart from the first package face (56),
a board connecting post (70) extending from the interposer (64) proximate the
first end (66) and terminating at the first package face (56),
a support post (74) spaced apart from the board connecting post (70), the
support post (74) extending from the interposer (64) proximate the second end (68) and
15 terminating at the first package face (56), and
a bond site (78) formed on a surface of the interposer (64) opposite the support
post (74), at least one of the I/O pads (80) being electrically connected to the interposer (64) at
the bond site (78).
- 20 2. The semiconductor device package (50, 102) of claim 1, wherein the at least
one of the I/O pads (80) is wire bonded or tape bonded to the bond site (78).
3. The semiconductor device package (50, 102) of claim 2, wherein the at least
one of the I/O pads (80) is electrically connected to the interposer (64) at the bond site (78) by
25 a wire forming a wedge bond at the I/O pad (80) and a wedge bond at the bond site (78).
4. The semiconductor device package (50, 102) of claim 3, wherein the wire is
made from aluminum or aluminum base.

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5. The semiconductor device package (110) of claim 1, wherein the at least one of the I/O pads (80) is directly soldered to the bond site (78) for forming a flip-chip type connection.

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6. The semiconductor device package (50, 102, 110) of claim 2, wherein the molding compound (54) forms at least a portion of a second package face (58) adjacent to the first package face (56), and a side surface (124) of the board connecting post (70) adjacent an end surface (72) of the board connecting post (70) is visible at the second package face (58).

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7. The semiconductor device package (50, 102, 110) of claim 6, wherein a corner between the side surface (124) of the board connecting post (70) and the end surface (72) of the board connecting post (124) is removed to form a relief (128), the relief (128) having a height of between about 1 mil to about 2 mils measured from the end surface (72) of the board connecting post (124).

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8. The semiconductor device package (50, 102, 110) of claim 1, wherein each of the leads (60) is formed from a strip of material having a channel (82) disposed across the strip.

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9. The semiconductor device package (50, 102, 110) of claim 8, wherein the channel (82) is filled with the molding compound (54).

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10. A method of packaging a semiconductor device (14), the method comprising:
forming a lead frame (52, 100, 112) from electrically conductive material, the lead frame (52, 100, 112) including a plurality of leads (60), each of the leads (60) including:

an interposer (64) having opposing first and second ends (66, 68),

a board connecting post (70) extending from the interposer (64) proximate the first end (66), the board connecting post (70) having an end surface (72) distal from the interposer (64),

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a support post (74) spaced apart from the board connecting post (70) and extending from the interposer (64) proximate the second end (68), the support post (74) having an end surface (76) distal from the interposer (64), and

a bond site (78) formed on a surface of the interposer (70) opposite the support post (74);

supporting the end surfaces (72, 76) of the support post (74) and the board connecting
65 post (70); and

electrically connecting I/O pads (80) on the semiconductor device (14) to the bond sites
(78) while supporting the end surfaces (72, 76) of the support post (74) and the board
connecting post (70); and

covering at least a portion of the semiconductor device (14), and at least a portion of
70 the lead frame (52, 100, 112) with a molding compound (54) while supporting the end surfaces
of the support post (74) and the board connecting post (70).

11. The method of claim 10, wherein electrically connecting the I/O pads (80) to the
bond sites (78) includes:

75 wire bonding or tape bonding each I/O pad (80) to an associated bond site (78).

12. The method of claim 11, wherein the wire bonding each I/O pad (80) to an
associated bond site (78) includes:

wedge bonding a wire (18) to the I/O pad (80), and
80 wedge bonding the wire (18) to the bond site (78).

13. The method of claim 12, wherein the wire (18) is made of aluminum or aluminum
base.

85 14. The method of claim 10, wherein electrically connecting the I/O pads (80) to the
bond sites (78) includes:

directly electrically connecting the I/O pads (80) to the bond sites (78) to form a flip-
chip type connection.

90 15. The method of claim 10, wherein supporting the end surfaces (72, 76) of the
support post (74) and the board connecting post (70) includes:

adhering the end surfaces (72, 76) of the support post (74) and the board connecting
post (70) to a surface (94).

95 16. The method of claim 10, wherein the molding compound (54) forms at least a
portion of a first package face (56), and the end surfaces (72, 76) of the support post (74) and
the bond connecting post (70) are coplanar with the first package face (56).

17. The method of claim 16, wherein the molding compound (54) forms at least a
100 portion of a second package face (58) adjacent to the first package face (56), and a side surface
(124) of the board connecting post (70) adjacent the end surface (72) of the board connecting
post (70) is visible at the second package face (58).

18. The method of claim 17, wherein a corner between the side surface (124) of the
105 board connecting post (70) and the end surface (72) of the board connecting post (70) is
removed to form a relief (128), the relief (128) having a height of between about 1 mil to about
2 mils measured from the end surface (72) of the board connecting post (70).

19. The method of claim 10, wherein forming the lead frame (52, 100, 112) includes:
110 forming a lead frame precursor from electrically conductive material, the lead frame
precursor including a plurality of lead precursors, each of the lead precursors being a strip of
the conductive material; and
disposing a channel (82) across each of the lead precursors to form the plurality of
leads (60).

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20. The method of claim 19, further comprising:
filling the channel (82) in each lead with the molding compound (54).

21. A semiconductor device package (50, 102, 300) comprising:
120 a molding compound (54) forming at least a portion of a first package face (56);
a semiconductor device (14) at least partially covered by the molding compound (54);
the semiconductor device (14) including a plurality of I/O pads (80); and
a lead frame (52, 100, 302) of electrically conductive material at least partially covered
by the molding compound (54), the lead frame (52, 100, 302) including a plurality of leads
125 (60), each of the leads (60) including a bond site (78) formed thereon, each bond site (78)
being electrically connected to an associated I/O pad (80) by a wire (18), the wire (18) forming
a wedge bond at the I/O pad (80) and a wedge bond at the bond site (78).

22. The semiconductor device package (50, 102, 300) of claim 21, wherein the wire
130 (18) is made from aluminum or aluminum base.

23. The semiconductor device package (50, 102) of claim 21, wherein each of the leads (60) further includes:

an interposer (64) having opposing first and second ends (66, 68), the interposer (64) being spaced apart from the first package face (56),

a board connecting post (70) extending from the interposer (64) proximate the first end (66) and terminating at the first package face (56),

a support post (74) spaced apart from the board connecting post (70), the support post (74) extending from the interposer (64) proximate the second end (68) and terminating at the first package face (56), the bond site (78) being formed on a surface of the interposer (64) opposite the support post (74).

24. The semiconductor device package (300) of claim 21, wherein the lead frame (302) is etched to separate the leads (60) after the molding compound (54) is applied to the lead frame (302).

25. The semiconductor device package (50, 102, 300) of claim 21, wherein the wire (18) has a wedge width between about 1.2 to about 1.5 times a diameter of a portion of the wire (18) extending between the I/O pad (80) and the bond site (78).

26. A method of packaging a semiconductor device (14), the method comprising: forming a lead frame (52, 100, 302) from electrically conductive material, the lead frame (52, 100, 302) including a plurality of leads (60), each of the leads (60) including a bond site (78) formed thereon;

electrically connecting I/O pads (80) on the semiconductor device (14) to the bond sites (78), the electrically connecting including:

wedge bonding a wire (18) to the I/O pad (80), and

wedge bonding the wire (18) to the bond site (78).; and

covering at least a portion of the semiconductor device (14), and at least a portion of the lead frame (52, 100, 302) with a molding compound (54).

27. The method of claim 26, wherein the wire (18) is made of aluminum or aluminum base.

28. The method of claim 26, wherein each lead includes:

an interposer (64) having opposing first and second ends (66, 68),
a board connecting post (70) extending from the interposer (64) proximate the first end (66), the board connecting post (70) having an end surface (72) distal from the interposer (64),
a support post (74) spaced apart from the board connecting post (70) and extending
170 from the interposer (64) proximate the second end (68), the support post (74) having an end surface (76) distal from the interposer (64), the bond site (78) being formed on a surface of the interposer (70) opposite the support post (74), the support post (74) supporting the bond site (78) during the wedge bonding of the wire (18) to the bond site (78).

175 29. The method of claim 26, wherein the wedge bonding includes ultrasonic bonding.

30. The method of claim 26, wherein the wedge bonding includes thermosonic bonding.

180 31. The method of claim 26, wherein the wire (18) is wedge bonded to the I/O pad (80) before the wire (18) is wedge bonded to the bond site (78).

32. The method of claim 26, further comprising:

185 etching the lead frame (302) to separate the leads (60) after electrically connecting the I/O pads (80) on the semiconductor device (14) to the bond sites (78).

33. The method of claim 26, wherein the wire (18) has a wedge width between about 1.2 to about 1.5 times a diameter of a portion of the wire (18) extending between the I/O pad (80) and the bond site (78).

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